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DESIGN AND PERFORMANCE EVALUATION OF A 200 °C INTERLEAVED BOOST CONVERTER (PREPRINT)

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14. ABSTRACT
Recent advances in SiC power semiconductor technology and resulting availability of SiC Schottky rectifiers and controlled devices (BJTs, JFETs, and MOSFETs) make it possible to design and implement power converters capable of operating at 200°C. The design, prototype development, operation, and testing of a 74 kHz, 2 kW, 100 V/270 V inversely-coupled, interleaved, dc-dc boost converter over the 20°C to 200°C temperature range is presented in this paper. The advantages of coupled-inductor interleaved boost converters include increased efficiency, reduced size, reduced electromagnetic emission, faster transient response, and improved reliability. Optimization of a high temperature X-perm core based coupled inductor architecture, in terms of ac flux balancing and dc flux cancellation is discussed. DC characterization of SiC power devices used in the design (Schottky rectifier and JFET) over the 20°C to 200°C temperature range is presented as well. The power stage of the converter, including the power semiconductor devices, coupled inductor, and X7R ceramic input and output filter capacitors, was placed inside a temperature controlled chamber for testing. JFET gate drive circuit, input power source, and output load were external to the environmental chamber. Converter testing and performance evaluation was accomplished over a 20°C to 200°C ambient temperature range. As expected, JFET conduction loss increased and converter efficiency decreased with increasing temperatures. The drop in converter efficiency was in the range of 2-4% over the entire load (200W to 2 kW) and temperature (20°C to 200°C) ranges evaluated. At 200°C, output voltage ripple increased by ~60% due to the rapid decline in X7R capacitance at the high temperature extreme. The results obtained during this study suggest that the realization of 200°C power converters is feasible through a judicious selection of power semiconductor devices, magnetic core materials, and capacitor dielectrics.

15. SUBJECT TERMS
power electronics, boost converter, interleaved, coupled inductor

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Design and Performance Evaluation of a 200°C Interleaved Boost Converter

Hiroyuki Kosai, James Scofield, Seana McNeal, Brett Jordan, *Member, IEEE*, and Biswajit Ray, *Member, IEEE*

***Abstract*— Recent advances in SiC power semiconductor technology and resulting availability of SiC Schottky rectifiers and controlled devices (BJTs, JFETs, and MOSFETs) make it possible to design and implement power converters capable of operating at 200°C. The design, prototype development, operation, and testing of a 74 kHz, 2 kW, 100 V/270 V inversely-coupled, interleaved, dc-dc boost converter over the 20°C to 200°C temperature range is presented in this paper. The advantages of coupled-inductor interleaved boost converters include increased efficiency, reduced size, reduced electromagnetic emission, faster transient response, and improved reliability. Optimization of a high temperature X-perm core based coupled inductor architecture, in terms of ac flux balancing and dc flux cancellation is discussed. DC characterization of SiC power devices used in the design (Schottky rectifier and JFET) over the 20°C to 200°C temperature range is presented as well. The power stage of the converter, including the power semiconductor devices, coupled inductor, and X7R ceramic input and output filter capacitors, was placed inside a temperature controlled chamber for testing. JFET gate drive circuit, input power source, and output load were external to the environmental chamber. Converter testing and performance evaluation was accomplished over a 20°C to 200°C ambient temperature range. As expected, JFET conduction loss increased and converter efficiency decreased with increasing temperatures. The drop in converter efficiency was in the range of 2-4% over the entire load (200W to 2 kW) and temperature (20°C to 200°C) ranges evaluated. At 200°C, output voltage ripple increased by ~60% due to the rapid decline in X7R capacitance at the high temperature extreme. The results obtained during this study suggest that the realization of 200°C power converters is feasible through a judicious selection of power semiconductor devices, magnetic core materials, and capacitor dielectrics. As a result, high temperature, frequency, and power density converters are expected to be a reality in the near future.**

Index Terms— SiC, Interleaved boost converter, coupled inductor, high temperature, DC/DC Converter

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I. INTRODUCTION

High temperature electronics are becoming increasingly important [1] in a multitude of applications including automobiles (on-engine and in-transmission environments), well drilling (instrumentation and localized drive electronics for oil and gas recovery), and aircraft and spacecraft (turbine engines, motor drives, and space propulsion systems). Advances in silicon-on-insulator (SOI) technology [2] and the steady development of wide bandgap semiconductors, such as silicon carbide (SiC), are enabling the practical deployment of high temperature electronics in the near future [3,4]. As temperature increases in a semiconductor, intrinsic carrier density increases, thereby increasing the leakage current. Additionally, device parameters vary, dielectric breakdown strength decreases, and coefficient of thermal expansion mismatches stress the die mechanically. Even with the use of SOI technology, these effects limit the maximum ambient use temperature of Si power devices to about 175°C. Above 175°C, use of wider bandgap semiconductor materials become imperative since they produce smaller concentrations of intrinsic carriers at elevated temperatures. Among the candidate wide bandgap materials, SiC device technology is perhaps the most promising, and certainly the most mature. SiC Schottky diodes are commercially available, and SiC BJTs [5,6], JFETs [7], and MOSFETs [8,9] are now transitioning from developmental to commercial market. In the passive components domain, X-perm ferrite material [10] is capable of high temperature operation, and the development of high temperature capable capacitors, with acceptable drop in capacitance value and decrease in leakage currents, is ongoing [11].

Previous studies have reported high temperature operation of SiC diodes, BJTs, JFETs, and MOSFETs [12,13] as well as power stages utilizing these devices [14,15]. However, the focus of this paper is the design, implementation, and testing of a 74 kHz, 2 kW, 100 V/270 V interleaved dc-dc boost converter (IBC) suitable for operation from 20°C to 200°C. A brief introduction to interleaved boost converter operation, along with optimization of the coupled inductor architecture in terms of ac flux balancing and dc flux cancellation, is presented in the following section. Magnetic properties of the high temperature X-perm core are reviewed, followed by the dc characterization of SiC power devices (JFETs and Schottky rectifiers) used in the converter design. Development of the converter prototype for high temperature testing is discussed, followed by the presentation of experimental results as a function of temperature. Finally, variation of converter efficiency, JFET conduction loss, and converter output voltage ripple over the 20°C to 200°C temperature range is presented.

II. INTERLEAVED BOOST CONVERTER

Interleaved buck and boost converters have been studied in recent years with the goal of improving power converter performance in terms of efficiency, size, conducted electromagnetic emission, and transient response. The benefits of interleaving include high power capability, modularity, and improved reliability. Since the inductor is frequently the largest and heaviest component in a power boost converter, the use of a coupled inductor instead of multiple discrete inductors is potentially advantageous. Coupled inductors also offer additional benefits such as reduced core and winding loss, as well as improved input and inductor current ripple. Generalized steady state analysis of multiphase interleaved boost converters has been previously reported [16]. Useful design equations for continuous inductor current mode (CICM) operation of an interleaved boost converter, including the effects of inductor coupling on the key converter performance parameters (inductor ripple current, input ripple current, and minimum load current requirement for achieving CICM operation), are detailed in [17]. Reports studying specific applications for coupled inductor topologies including soft switching, active clamping, and high power utilization are becoming more prevalent in the literature as understanding of their benefits increase [18, 19, 20, 21, 22].

The schematic of an inverse-coupled interleaved boost converter topology is shown in Fig. 1. For the coupled inductor, the mutual inductance is *M* and the self inductances (L_1 and L_2) are assumed to be equal with a value of *L*, and the coupling factor (*k)* defined as *M/L*. A set of theoretical waveforms for CICM operation of the interleaved boost converter is shown in Fig. 2 for a duty ratios (*D*) greater than 0.5. Applying volt-sec balance to either winding of the coupled inductor provides the well-known dc voltage gain equation [$V_{out}/V_{in} = 1/(1-D)$].

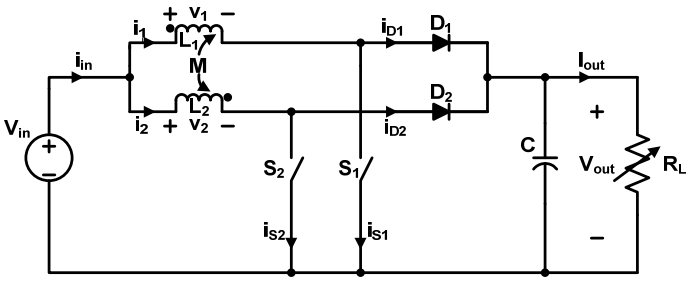


Fig. 1. Inverse-coupled interleaved boost converter topology.

A. The Coupled Inductor

Intentional core gaps are the main source of leakage flux in the energy storing inductor. Outside the windings, flux associated with leakage takes a shorter path (i.e. through the air) and is therefore uncoupled. Flux associated with mutual inductance travels through both set of windings, a large portion of which remains in the core. In the dc

environment, where two windings share the dc current equally, a flux-cancelling inverse-coupled configuration is utilized by implementing windings having opposing polarity. At the core directly underneath the windings of N turns each, the resultant flux is $(1-k)LI_{dc}/N$, where I_{dc} is dc current through the winding. Thus, an inverse coupled inductor winding results in a much more compact geometry as dc flux saturation is avoided.

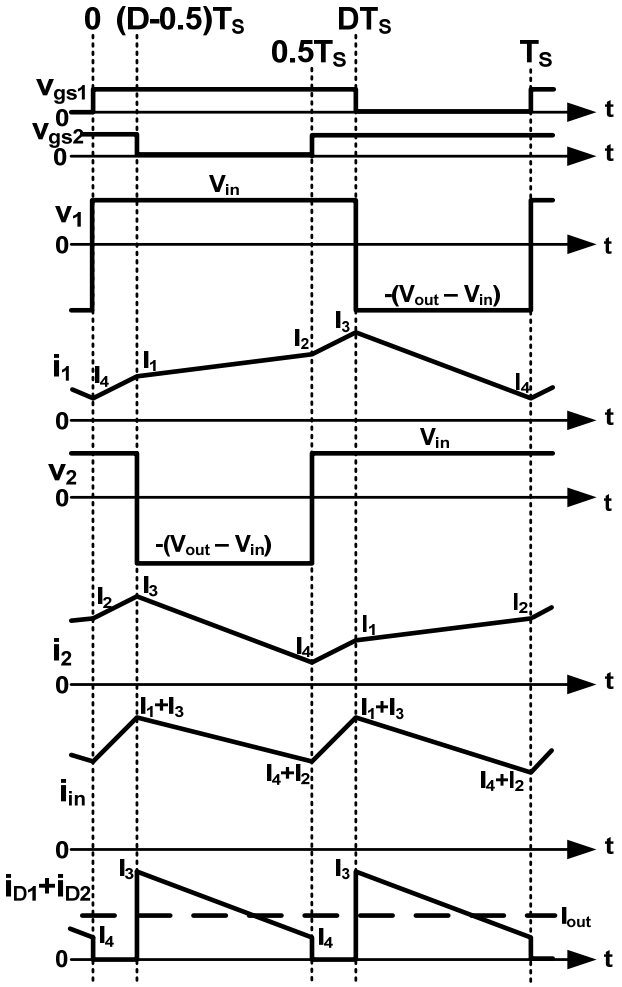


Fig. 2. Steady state waveforms of the interleaved boost converter under CICM operation (D > 0.5).

B. Magnetic field and dc flux simulation for the coupled inductor

Table I lists design parameters for three coupled inductor configurations considered, with gaps adjusted to generate similar *k*-values and windings were scaled so that the inductances closely matched. Fig. 3 illustrates the geometries and winding configurations [23].

Using the inductor parameters of Table I, finite element solid models were created in *QuickField 5.6*, and used to perform two groups of simulations for performance comparison. One ampere-turn winding excitation was used for all computations of dc flux distributions in the inverse coupled inductor models. The first simulations utilized physical models reflecting the tested inductors' measured geometries and permeabilities. The second simulation group consisted of modifying the physical models to equalize cross sectional areas, permeabilities, gap length, and magnetic flux path lengths of the E-E and 45° gap core inductors to that of the square 90° gap core inductor model. Since there are four gaps for both the 45° and the 90° core inductor, the two outer leg gaps of the E-E core were set to twice the gap dimension of the other two inductors. Fig. 4 shows the simulated dc flux density characteristics of the three coupled inductor models during inversely coupled operation with one ampere-turn input. As can be seen in Fig. 4, the E-E core produced the highest peak and average value of flux density of the three cores considered. Only a 0.2 G difference was predicted between the peak flux values of the two square cores, with the 90° gap core yielding the lowest predicted flux density. From these simulations, verification of significant dc flux cancellation in inverse coupled configurations is confirmed, as is the apparent superiority of square geometries.

These modeled flux distribution results provide further evidence of the suitability of an inverse coupled winding configuration for high power interleaved boost converters. In addition, these results highlight the potential benefit that coupled inductor boost converters offer in terms of reduced magnetic component volume and weight. Additionally, a peak dc flux density comparison was carried out for one-leg and two-leg (interleaved) operation of the magnetic core. For simulation purpose, a one-turn coil was excited by 1 A of dc current per Fig. 3 (right most winding and core configuration). The corresponding flux density distribution is shown in Figs. 5 and 6 for one-leg and two-leg operation of the magnetic core, respectively. The air gap between core sections was assumed to be 1 mm for the simulation. It can be seen from Figs. 5 and 6 that the peak flux densities are approximately 1 mT and 0.08 mT for one-leg and two-leg operations, respectively. Thus, for a 9-turn winding carrying 18 A of dc current

TABLE I
INDUCTOR PARAMETERS

Inductor type	# of turns per leg	Air gap (mm)	L (μH)	M (μH)	k	μ_r
E-E core	14	3.4	33.6	23.1	0.69	1680
Square 90° gap	20	1.6	35.9	25.4	0.71	500
Square 45° gap	16	2.8	32.4	20.1	0.64	2500

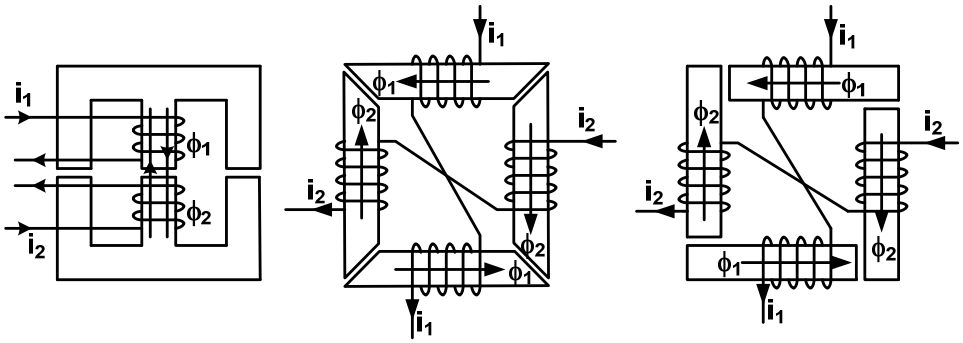


Fig. 3. Winding configuration of the coupled inductors. (L to R: E-E core, square 45° gap core, and square 90° gap core)

(corresponding to about 2 kW of output power for the dc-dc converter), the peak flux densities are approximately 162 mT and 13 mT for one-leg and two-leg operations, respectively. Since the saturation flux density of the X-perm core used in designing the coupled inductor is 200 mT (= 2000 Gauss) at 250°C, it can easily be operated at 200°C ambient in a two-leg (interleaved) configuration. One-leg operation of the core on the other hand is possible; however, the associated flux density margin may not be sufficient for many applications. Finally, the simulated self-inductance value was calculated to be 43.5 μH which compares reasonably well to the measured value of 39.8 μH. This discrepancy between simulated and experimental values is consistent with the three-dimensional flux leakage unaccounted for in two-dimensional modeling software. In summary, an interleaved boost converter implemented in a two-leg configuration using a high-temperature magnetic core can be successfully operated at 200°C with a

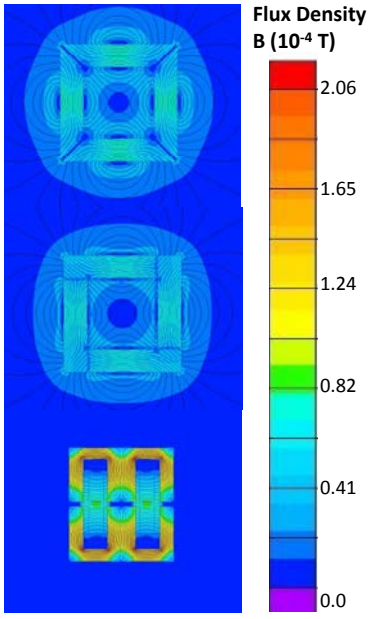


Fig. 4: Flux density map for normalized inductor models. (Top to Bottom: square 45° gap core, square 90° gap core, and E-E core)

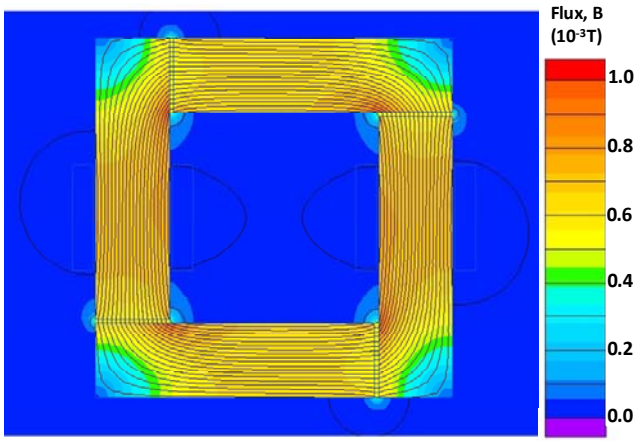


Fig. 5. Magnetic flux density distribution in the core for one-leg operation.

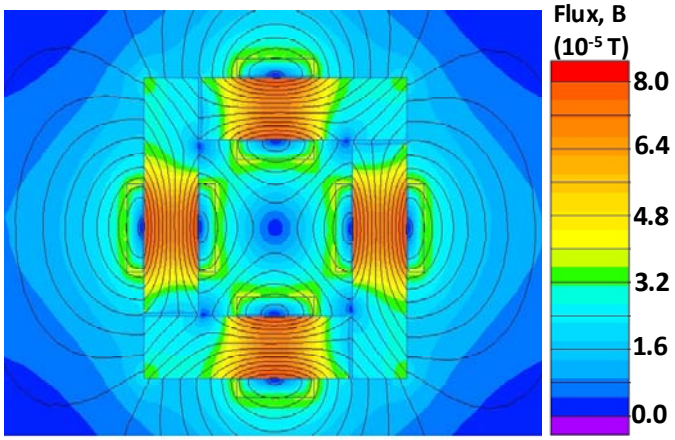


Fig. 6. Magnetic flux density distribution in the coupled-inductor core for two-leg operation.

significant flux density design margin, whereas this is not a possibility in a single-leg configured inductor.

C. Magnetic Core Material

An X-perm core made of a Fe-Mn-Zn ferrite material, with a Curie temperature in excess of 300°C [10], was used in constructing the coupled inductor. A square core with 90° gap was created using four rectangular pieces as shown in Fig. 3 (right most diagram). Key magnetic properties of the X-perm high temperature material are: relative permeability of 500-1000 at 25°C, saturation flux density of 0.48 T at 25°C/0.3 T at 200°C/0.1 T at 300°C, coercive force of 0.5 Oe at 25°C and 0.35 Oe at 200°C, power loss of less than 1 W/cm^3 @200 kHz/0.08 T, and a resistivity of 100-200 Ω·cm. The temperature dependent permeability, saturation flux density, and core loss data used for the X-perm inductor core design were obtained from the manufacturer's measurements [10].

D. SiC Power Semiconductor Selection

The power semiconductors used for designing the power stage are shown in Table II. The enhancement mode silicon carbide JFET [24] has the advantages of no saturation voltage (unipolar mode operation), no tail-current, low on-resistance (100 mΩ), low intrinsic capacitance, and positive temperature coefficient. Even though the normally-off JFET doesn't require negative bias for full blocking, in practice a negative off-state voltage (in the range of -5 to -15 V) is used since the gate threshold voltage can be as low as 750 mV. Use of a negative gate bias provides improved noise immunity as well as shorter turn-off times. In addition, VJFET's do not have an intrinsic body diode between source and drain and switching transients that might bias the device into reverse conduction serve to increase the n-channel resistance. Thus to minimize high frequency operation switching losses, SiC Schottky devices are used as anti-parallel diodes in our circuit. Specific gate drive considerations for the normally-off SiC JFETs are dynamic charging/discharging of the total gate capacitance (similar to MOSFETs) and a continuous current through the gate-source diode during the entire on-period (similar to BJTs). Typically, a modest gate current of 200 mA, corresponding to a gate-source voltage of about 3 V, is nominally adequate for these 15 A rated parts. Additional increases in gate current or gate-source voltage do not yield further reduction in $R_{DS,ON}$ and unnecessarily increases gate drive power requirements. For high temperature applications, the dependence of $R_{DS,ON}$ with temperature is a key parameter. From the JFET data sheet, $R_{DS,ON}$ increases by a factor of 2.2 as temperature is increased from 25°C to 125°C. Figure 7 shows normalized data sheet and rapid I-V measured drain-to-source $R_{ds,on}$ values as a function of temperature. The gate-bias and drain current conditions for the measurements are listed in

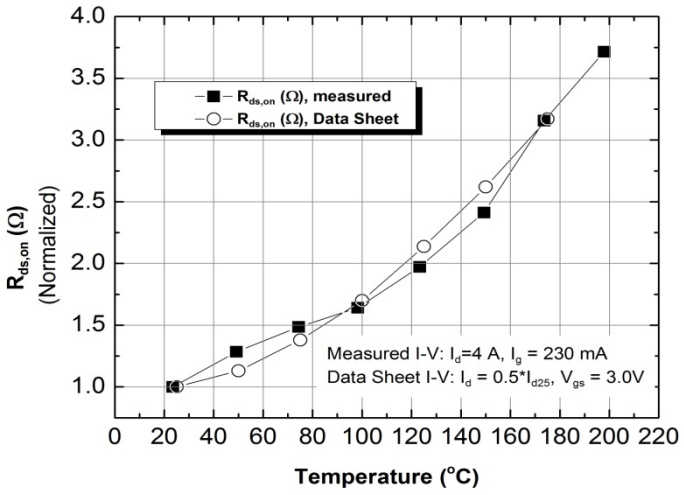


Fig. 7. Normalized drain-to-source on-resistance of an enhancement mode SiC JFET measured (I_d = 4 A, I_g = 230 mA), and Data Sheet values (Id=0.5I_{d25}, Vgs = 3.0 V).

the plot inset. The data reflects an increase of $R_{DS,ON}$ by a factor of ~2.0 over the 25°C to 125°C range and by a factor of 3.75 at 200°C, and is seen to be consistent with the manufacturers data.

For converter output rectification and free-wheeling diode function, low V_F 300V SiC Schottky diodes from Cree, Inc. were used for the 270V output converter. Use of 600 or 1200 V diodes would increase conduction losses unnecessarily, although JFETs are available only in the higher voltage rating (1200 V). As with JFET V_{DS}, the diodes positive temperature coefficient of V_F makes these devices very amenable to paralleling in order to achieve high current handling capability. Figure 8 shows the forward voltage drop of a 300 V Schottky as a function of temperature for a forward current of 6.5 A as measured on a hotplate with a pulsed curve tracer excitation. Also shown for comparison is the 6.5 A V_F data from the manufacturer's curves reflecting that our measured resistance is nominally within the 10% range specified on the data sheet. The positive temperature coefficient, associated with acoustic phonon carrier scattering limited mobility is evident.

TABLE II
SiC POWER SEMICONDUCTOR DEVICES USED IN PROTOTYPE DEVELOPMENT

Device reference designator	Device type	Part #	Key specifications
S_1, S_2	Normally -off JFET	SJEP120R125 (SemiSouth)	1200 V, 15 A, $R_{DS,ON}$=0.125 Ω, T_j=175°C, TO-247
D_1, D_2	Schottky rectifier	CSD20030 (Cree Inc.)	300 V, 20 A, V_F=1.4 V @10 A, T_j=175°C, TO-247

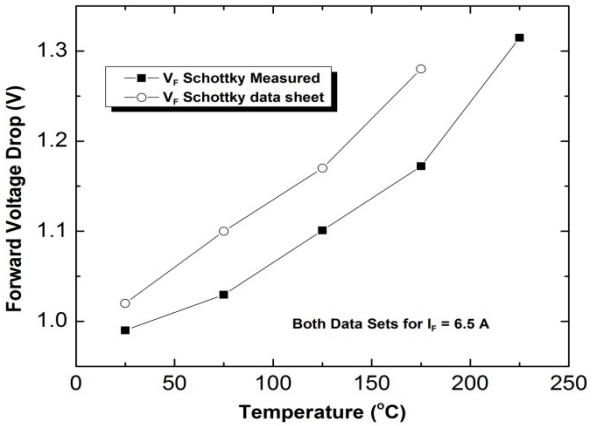


Fig. 8. SiC diode forward voltage drop as a function of temperature (I_F = 6.5 A). Measured and data sheet curves.

E. Capacitor Selection

For higher dielectric constant capacitors such as ceramics, capacitance generally decreases and leakage current increases with increasing temperatures. For low capacitance values, C0G (Class I) ceramic capacitors are likely the best choice due to lower dissipation factor and stable temperature characteristics. However, due to the requirement for converter output capacitance values in the range of 30-60 μF for this design, X7R (Class II) ceramic capacitors are the next best alternative. The input filter capacitance consisted of a single 30 μF/300 V/X7R (AVX) capacitor. The output filter capacitance of 60 μF consisted of two 30 μF/300 V/X7R (AVX) capacitors. It shall be noted that the capacitance of stacked MLC capacitors drops significantly in value between 125°C and 200°C [25] and results in degraded output ripple performance at the higher temperatures tested.

III. CONVERTER PROTOTYPE DEVELOPMENT

An interleaved dc-dc boost converter was prototyped and tested to verify its successful operation from room temperature (20°C) up to 200°C. Each leg of the interleaved converter consisted of three SiC JFETs (SJEP120R125) and three SiC Schottky diodes (CSD20030). Each side of the 90°-cut square coupled inductor consists of a 22 mm x 17.6 mm x 67.3 mm rectangular X-perm core with an airgap of 0.7 mm between sections. Each section of the inductor core possessed 9 turns of 2.54 cm x 0.05 cm Kapton insulated copper tape for the windings, resulting in 18 turns per converter leg (see the right most diagram of Fig. 3). Self and mutual inductances and coupling factor of the fabricated inductor (39.8 μH, 25.6 μH, and 0.64, respectively) were obtained by alternately opening and shorting the secondary winding leads and using an HP4284A LCR meter for measurement. In terms of the input and output filter capacitors, an output capacitance of 60 μF (2*30 μF, 300V, X7R) and an input capacitance of 30 μF (1*30 μF, 300 V, X7R) were used. Converter assembly was done with careful attention paid to the layout symmetry of each leg of the prototype, especially the inductor windings and JFET switching sections, to minimize differences in parasitic impedance and help achieve balanced current sharing for each phase.

All power stage components of the converter were placed inside the environmental chamber. The JFET gate drive circuit, DC power supplies, and resistive load bank, were placed outside the thermal chamber with gate-source signals connected to the JFET pins via high temperature coaxial cables (200°C; MIL-C-17D VW-1, 0.6m long, 50Ω, RG 188A/U) and heavy Cu braid provided the source and load connections. The gate signal generation circuit consisted of a PWM IC (SG3525A) followed by a high current driver IC (TC4421A). Gate current during the on-period was maintained at approximately 100 mA per device by adjusting the positive bias of an optocoupler IC

(HCPL3180). The measured gate current during switching transitions was approximately 200 mA per device. The gate drive circuit was not optimized to provide increased current during the switching transitions, typically needed for high frequency applications. This was found not to be an issue for the 74 kHz switching frequency application presented herein. Converter efficiency presented in the next section is for the power stage only, i.e., the estimated 255 mW/device gate power loss would serve to very slightly decrease those numbers.

All internal electrical connections for the power stage of the prototype were either high temperature solder (240°C liquidus temperature; 95Sn/5Sb) or metal screws and nuts. Copper plates were used as power and ground planes to achieve a low-resistance and low-inductance converter prototype. Kapton® polyimide film tape was used as the insulating material (rated for 260°C) for inductor core encapsulation, support chassis and ground plane insulation, inductor winding ribbon insulation, and wire insulation for the DC bus supply and from output to load bank. Figure 9 shows a picture of the prototype converter prior to assembly in the environmental chamber.

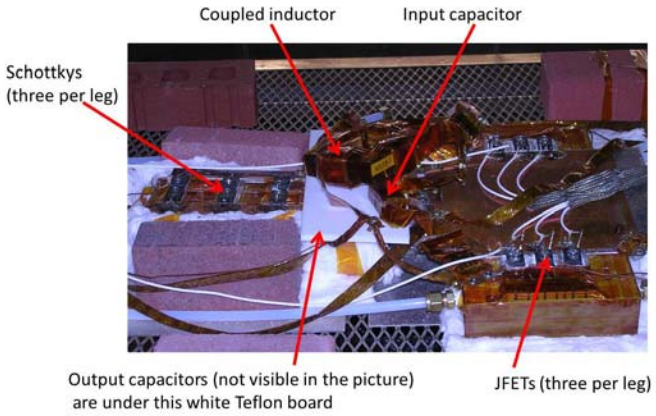
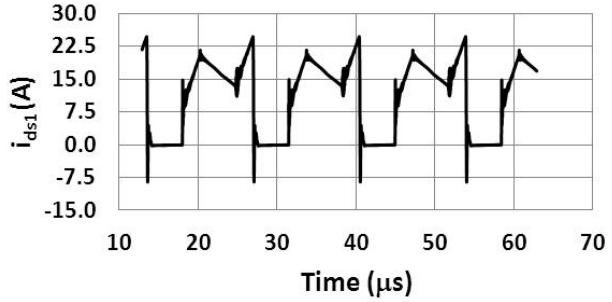


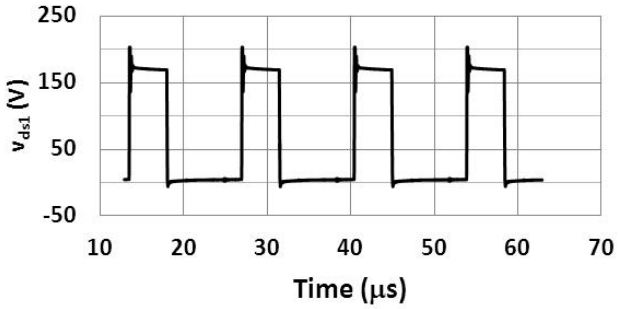
Figure 9. Interleaved converter prototype sections prior to assembly in environmental chamber.

IV. EXPERIMENTAL RESULTS

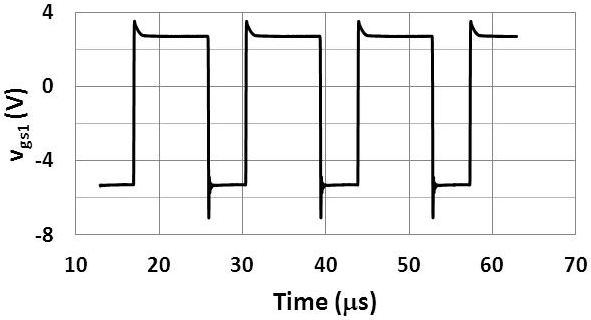
Each leg of the converter was switched at a frequency of 74 kHz with a phase shift of 180° between the two legs. The converter was operated over a load range of 200 W to 2 kW with a fixed switch duty ratio of 0.66, corresponding to a theoretical dc voltage gain of 2.94. The input voltage was varied between 20 and 60 V while the load resistance varied between 8 Ω and 16 Ω to achieve the desired output power. A set of recorded waveforms (combined current through the JFETs, drain-to-source voltage, and gate-to-source voltage) at room temperature (20°C) is shown in Figures 10 for one of the two phase legs of the interleaved converter. Reasonably balanced current sharing between the two interleaved legs was verified by comparing the current waveform data like that shown in Fig.10 for both switch positions.



(a) Drain current of S_1



(b) Drain-to-source voltage of S_1



(c) Gate-to-source voltage of S_1

Fig. 10. Recorded converter waveforms of Leg-1 at 20°C. (V_{in} = 60 V, R_L = 16 Ω, P_{out} = 1.85 kW).

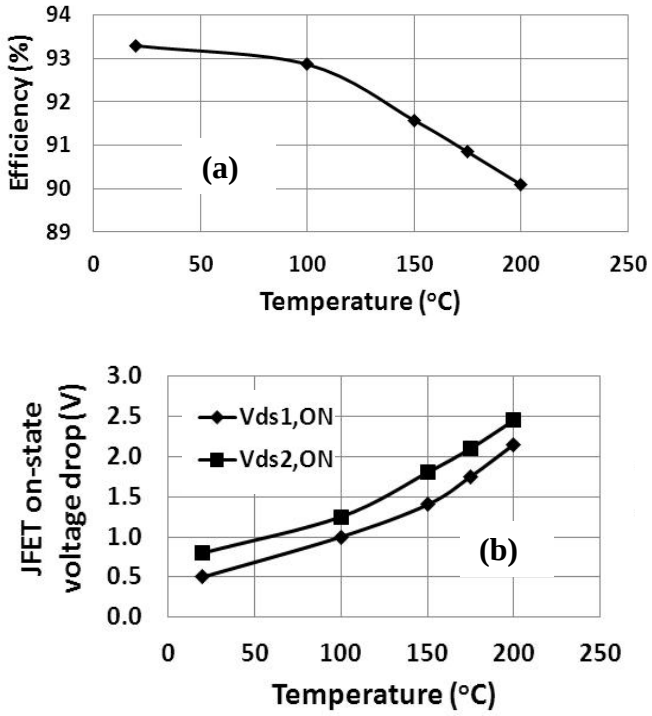
Current balance was achieved by careful layout and symmetry considerations of the converter hardware since the converter was operated without gate feedback control. Furthermore, since the converter is operated in a hard-switching PWM mode, dynamic noise at turn-on and turn-off transitions is expected and can also be seen in the waveforms of Figure 10. The switching noise at turn-off is higher than at turn-on, primarily due to layout inductance in the SiC diode and JFET loop (including the device package inductances). The long cable connecting the output of the optocoupler IC (located outside the temperature chamber) to the gate-source pins of the JFET (located inside the temperature chamber) also contributed to the modest converter switching noise seen in Fig. 10.

However, it was possible to significantly reduce the converter's switching noise contribution to the larger power system by the appropriate use of common-mode chokes as part of the converter's input and output filters. In addition, measurements made in the environmental chamber utilized dedicated high temperature coaxial lines connected directly to the JFET g-d-s terminals for oscilloscope connection. This configuration, coupled with the high input impedance of the oscilloscope, enabled accurate current waveform records and JFET $V_{DS}(T)$ measurements in spite of the ~0.6 meter length between gate driver board and JFET switches as seen in Fig 10.

Once room temperature performance was successfully evaluated, the power section of the converter was operated at successively higher temperatures with dc performance data recorded at ambient oven temperatures of 100°C, 150°C, 175°C, and 200°C. Although JFET and Schottky diode plastic injection molded TO-247 packaging is nominally rated to only 175 °C device junction temperatures, we have successfully used these packages at elevated temperatures in several prototype converter components for durations of up to 100 hours. While not expected to provide long term reliability or extended life expectancy, it has been found that these packaged devices are satisfactory for prototyping the performance characteristic benefits of SiC. For applications in which longer life operation is desired, SiC die are brazed in metal TO-257 hermetic packages, which do provide superior high temperature reliability.

With no external forced or compressed air cooling, the experimentally measured JFET case and heat sink temperatures were typically 10-15°C above the oven temperature at 1.85 kW of converter output power. Due to a lack of high temperature probes, only the JFET terminal characteristics were measured under heated chamber conditions. Load and input powers were measured at the chamber entry/exit lugs. The converter efficiency as a function of oven temperature is shown in Figures 11(a) and 12(a) for output power of 1 kW and 1.85 kW, respectively. The corresponding JFET on-state voltage drop and output peak-to-peak voltage ripple are shown in Figures 11 and 12 (b) and (c), respectively. It can be observed that the converter efficiency stays relatively unchanged from 20°C to up to about 100°C, and the monotonic drop in efficiency from 100°C to 200°C totals approximately 2-3%. This is consistent with the increase in JFET on-state voltage with increased temperature as seen in Figures 11(b) and 12(b). The approximate doubling of JFET on-state voltage from 100°C to 200°C corresponds to a commensurate increase in switch conduction loss. Finally, the output ripple voltage increase with increasing temperatures was expected due to the ~50% X7R capacitance decrease from 25°C to 200°C, as shown in Figure 13 [11, 25]. Output ripple voltage is dictated by two factors: filtering effect of the capacitor (i.e., its charging

and discharging) and the ac voltage drop across its ESR. Due to the drop in output capacitance value with temperature, the 200°C ripple voltage was expected to increase significantly compared to its room temperature value. As seen in Figures 11(c) and 12(c), the output ripple voltage at 200°C is 55-60% higher than the 20°C value. A *PSpice* simulation was carried out to validate the measured output voltage ripple with X7R characteristics based on datasheet characteristics. The capacitance was assumed to vary with temperature per Fig. 13, with ESR fixed at 18 mΩ. The simulated and experimental output voltage ripple data, compared in Fig. 14, are highly correlated. For the simulation, ESR was assumed to be independent of temperature [26], however, it is expected to be temperature dependent since capacitor dielectric properties are temperature dependent. The simulation and experimental data matched well for the fixed ESR assumption since the contribution of ESR to overall output voltage ripple is generally not significant for ceramic capacitors. For a 16 Ω/1.85 kW load, the resulting temperature-independent capacitor RMS current of 8.76 A corresponds to a power loss of 1.38 W. Thus each of the 30 μF output capacitors dissipates 690 mW, resulting in a relatively small increase in its operating temperature due to internal heating.



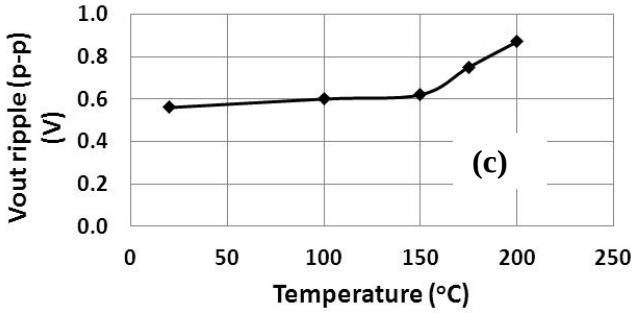
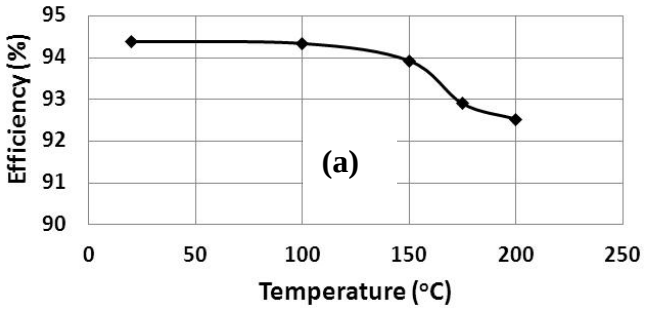
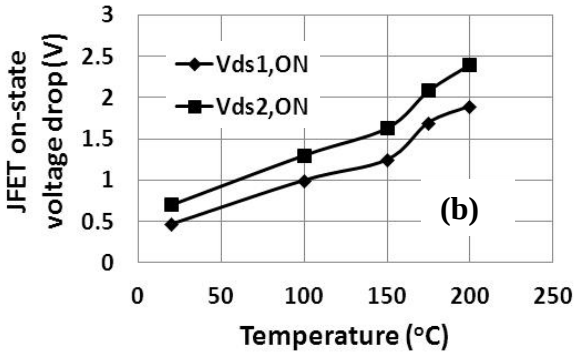


Fig. 11. Interleaved converter performance as a function of temperature.
(V_{in} = 33 V, R_L = 8 Ω, P_{out} = 1 kW). (a) Efficiency, (b) JFET V_F, and (c) Output ripple voltage.





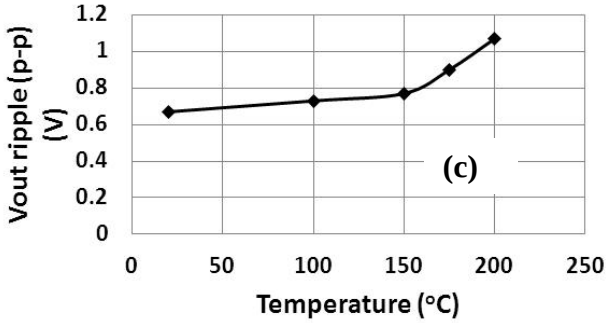


Fig. 12. Interleaved converter performance as a function of temperature.
(V_{in} = 60 V, R_L = 16 Ω, P_{out} = 1.85 kW).). (a) Efficiency, (b) JFET V_F, and (c) Output ripple voltage.

Measured converter efficiency as a function of temperature and output load is shown in Figure 15 for operation at 100°C, 150°C, and 200°C. As discussed earlier, for a given load condition, the converter efficiency is expected to drop with increasing temperatures; Figure 15 shows this drop in efficiency from 100°C to 200°C to be about 1.2% and 2.5% at 500 W and 800 W of operation, respectively. Thus the efficiency drop data is consistent among Figures 11, 12, and 15. Similarly, for a given temperature, the converter efficiency is expected to drop with increasing load due to increased conduction loss in JFETs, rectifiers, and the coupled inductor. Based on Figure 15 and recorded experimental data, the drop in converter efficiency is between 2 and 4% as load varies from 200 W to 2 kW over the 20°-200°C range. Using the JFET on-state voltage data of Fig. 11b and 12b, together with the manufacturers I-V-T and $R_{ds,on}$(T) data sheet information and duty cycle (D=0.66) the IBC JFET currents and power losses can be estimated for each of the two interleaved converter legs. Table III summarizes the power dissipation estimates calculated for each converter leg and the total, including switching losses for 74 kHz operation using data sheet temperature dependent switching energy curves. The approximate equality of the total loss estimates, for 1 kW and 1.85 kW output power conditions, is due primarily to the equality of the load current in each case and the dominance of conduction compared to switching losses. In addition, the data sheet dynamic energy curves are provided only for Vds,off = 600 V and our two power levels were at ~100 V and 200 V, respectively. Thus, our switching energy estimates are very conservative with the 1.0 kW case overestimated a greater amount than the 200 V, 1.85 kW case. As seen from the individual boost leg power dissipation columns in Table III, a slightly unbalanced current condition between the two phase legs resulted in measurable differences in power dissipation per leg. In practice, this could create unbalanced temperature distributions between the two JFET switching sections exacerbating current imbalance issues, and potentially reliability. This highlights a problem when using open loop gate control

in an IBC, which is that at unexpectedly high temperatures the more resistive JFET phase leg may crossover into an undesirable bipolar operation mode. Thus, in practice, a more rigorous enhancement mode JFET gate control paradigm is required to ensure that temperature and bias voltage information are used to proactively adjust V_{GS} to remain below gate diode forward bias injection conditions. An approach similar to that proposed by Wrzecionko et. al. [27] would potentially be highly effective.

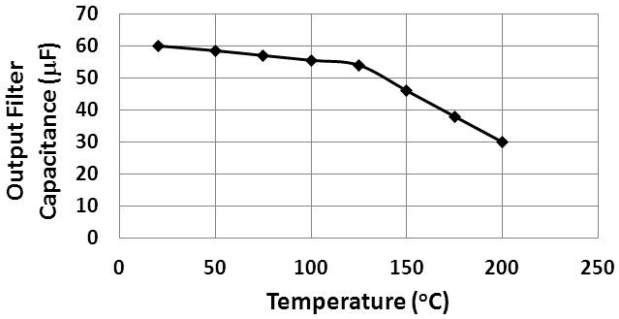


Fig. 13. Capacitance variation with temperature of the 60 μF output capacitor.

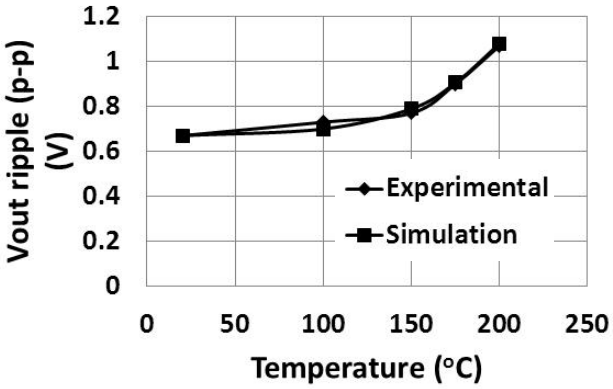


Fig. 14. Output ripple voltage (peak-to-peak) comparison.
(V_{in} = 60 V, R_L = 16 Ω, P_{out} = 1.85 kW)

V. CONCLUSIONS

Successful design, implementation, testing, and operation of an interleaved boost dc-dc power converter over a 20°C to 200°C temperature range have been presented. Optimization of the coupled inductor in terms of magnetic core architecture and dc flux cancellation is also discussed. Magnetic properties of high temperature X-perm cores and dc characterization of SiC power semiconductors, including Schottky rectifier and JFET switch, are reported as a function of temperature.

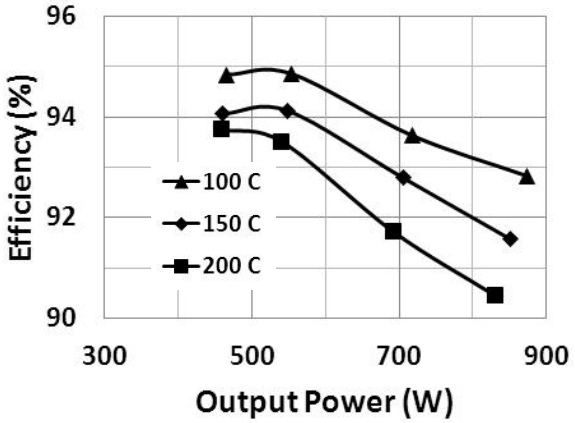


Fig. 15. Converter efficiency variation with output load and temperature (V_{in} = 30 V, V_{out} ≈ 84 V).

Table III. SiC JFET IBC Switch Loss Estimates

Power Loss / Temp	$P_{Leg1}tot$ (watt) 1 kW output	$P_{Leg2}tot$ (watt) 1 kW output	$P_{Leg1}tot$ (watt) 1.85 kW output	$P_{Leg2}tot$ (watt) 1.85 kW output	P_{total} Cond + switch 1 kW	P_{total} Cond + switch 1.85 kW
25°C	15.80	25.83	15.69	25.52	41.64	41.21
100°C	26.87	45.37	26.7	45.51	72.25	72.21
175°C	47.01	66.85	47.93	65.59	113.86	113.53

Implementation and layout of the prototype inside the temperature chamber are discussed in relation to high temperature testing of the converter. Experimental data over a wide load (200 W to 2 kW) and temperature (20°C to 200°C) range showed a 2 to 4% drop in efficiency. This relatively small drop in efficiency is primarily due to the selection and use of high temperature capable semiconductor devices as well as passive components (X-perm magnetic core and X7R capacitors). The output voltage ripple of the converter increased with increasing temperatures primarily due to a drop in X7R capacitance value. Until large-value temperature-stable capacitors (in tens of μF) are commercially available, the output ripple voltage requirement at 200°C will necessitate a continuation of the practice of overdesigning the room temperature output capacitance requirement. Due to fast switching, low on-resistance, low gate charge, and low junction capacitances of emerging SiC semiconductor devices, it is now feasible to design high power and high density converters suitable for high temperature operation for a variety of applications requiring high reliability, robust power supply performance.

VI. REFERENCES

1. H. Alan Mantooth et al., "Emerging capabilities in electronics technologies for extreme environments, Part I: High temperature electronics," IEEE Power Electronics Soc. Newsletter, Vol. 18, No. 1, pp. 9-14, Jan. 2006.

2. M. A. Huque et al., “Silicon-on-insulator based high-temperature electronics for automotive applications,” Proc. IEEE Int. Symposium on Industrial Electronics, pp. 2538-2543, June 2008.
3. J. Hornberger et al., “Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments,” Proc. IEEE Aerospace Conf., pp. 2538-2555, March 2004.
4. A. Hefner et al., “Emerging silicon-carbide power devices enable revolutionary changes in high voltage power conversion,” IEEE Power Electronics Soc. Newsletter, Vol. 16, No. 4, pp. 10-12, Oct. 2004.
5. S. Krishnaswami et al., “1000-V, 30-A 4H-SiC BJTs with high current gain,” IEEE Electron Device Letters, Vol. 26, No. 3, pp. 175-177, March 2005.
6. TranSiC, http://www.transic.com/index.php/products.
7. D. Peftitsis et al., “High-power modular multilevel converters with SiC JFETs,” Proc. IEEE Energy Conversion Congress & Exposition, pp. 2148-2155, Sept. 2010.
8. J. Scofield et al., “Performance and reliability characteristics of 1200 V, 100 A, 200^{o}C half-bridge SiC MOSFET-JBS diode power modules,” Proc. Int. Conf. High Temperature Electronics, Int. Microelectronics & Packaging Society, May 2010.
9. J. Wang et al., “10-kV SiC MOSFET based boost converter,” IEEE Trans. Industry Applications, Vol. 45, No. 6, pp. 2056-2063, Nov/Dec. 2009.
10. R. Spyker et al., “300C ferrite material for high temperature magnetics,” Proc. IEEE Power Electronics Specialists Conference, pp. 155-160, June 2004.
11. S. Harris, “Stacked-ceramic caps brave high temperatures,” Power Electronics Technology, pp. 38-40, Aug. 2007.
12. Powerex, Inc., Silicon carbide MOSFET Module (QJD1210007), www.pwrx.com/pwrx/docs/qjd1210007.pdf (datasheet).
13. Cree Inc., “CMF20120D-Silicon carbide Power MOSFET,” www.cree.com/products/pdf/**CMF20120D**.pdf (datasheet).
14. B. Ray, H. Kosai, J. Scofield, and B. Jordan, “200^{o}C operation of a dc-dc converter with SiC power devices,” Proc. IEEE Applied Power Electronics Conf., Feb. 2007.
15. K. Takao et al., “Performance evaluation of all SiC power converters for realizing high power density of 50 W/cm^{3},” IEEE Int. Power Electronics Conf., pp. 2128-2134, June 2010.
16. H. Shin et al., “Generalized steady-state analysis of multiphase interleaved boost converter with coupled inductors,” *IEE Proc. Elect. Power Appl.*, Vol. 152, No. 3, pp. 584-594, May 2005.
17. B. Ray et al., “A comprehensive multi-mode performance analysis of interleaved boost converters,” Proc. IEEE Energy Conversion Congress & Exposition, pp. 3014-3021, Sept. 2010.
18. Tsun-Hsiao Hsia; Hsien-Yi Tsai; Dan Chen; Lee, M.; Chun-Shih Huang; , "Interleaved Active-Clamping Converter With ZVS/ZCS Features," Power Electronics, IEEE Transactions on , vol.26, no.1, pp.29-37, Jan. 2011.

19. Dwari, S.; Parsa, L.; , "An Efficient High-Step-Up Interleaved DC–DC Converter With a Common Active Clamp," Power Electronics, IEEE Transactions on , vol.26, no.1, pp.66-78, Jan. 2011.
20. Sungsik Park; Yohan Park; Sewan Choi; Woojin Choi; Kyo-Beum Lee, "Soft-Switched Interleaved Boost Converters for High Step-Up and High-Power Applications," Power Electronics, IEEE Transactions on, vol.26, no.10, pp.2906-2914, Oct. 2011.
21. Jung, D.-Y.; Ji, Y.-H.; Park, S.-H.; Jung, Y.-C.; Won, C.-Y.; "Interleaved Soft-Switching Boost Converter for Photovoltaic Power-Generation System," Power Electronics, IEEE Transactions on , vol.26, no.4, pp.1137-1145, April 2011
22. Chen, Y.-T.; Shiu, S.; Liang, R.; "Analysis and Design of a Zero-Voltage-Switching and Zero-Current-Switching Interleaved Boost Converter," Power Electronics, IEEE Transactions on , vol.27, no.1, pp.161-173, Jan. 2012
23. H. Kosai et al., "Coupled inductor characterization for a high performance interleaved boost converter," IEEE Trans. on Magnetics, Vol. 45, No. 10, pp. 4812-4815, Oct. 2009.
24. SemiSouth Laboratories, Inc., http://www.semisouth.com/power-semiconductors
25. AVX Corp., "SMPS stacked MLC capacitors," www.avx.com/docs/Catalogs/smx.pdf (datasheet).
26. R. Tse et al., "ESR performance with temperature," TDK Components USA, Nov. 2006.
27. B. Wrzecionko, S. Kach, D. Bortis, J. Biela, J. Kolar, "Novel AC coupled gate driver for ultra fast switching of normally-off SiC JFETs", Proc. IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, pp.605-612, 7-10 Nov. 2010.